CLAIMS

The invention claimed is:

1. A semiconductor-on-insulator construction, comprising:

an electrically insulative material;

a crystalline layer comprising silicon and germanium over the electrically insulative material; and

a transistor device having a gate and an active region proximate the gate; the active region extending into the crystalline layer; the entirety of the active region within the crystalline layer being within only a single crystal of the crystalline layer.

2. The construction of claim 1 wherein the crystalline layer comprises from about 10 to about 60 atomic percent germanium.

3. The construction of claim 1 wherein the crystalline layer is polycrystalline.

4. The construction of claim 1 wherein the crystalline layer is monocrystalline.

5. The construction of claim 1 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the crystalline layer and the transistor device gate.

6. The construction of claim 5 wherein the strained crystalline lattice includes silicon.

7. The construction of claim 5 wherein the strained crystalline lattice includes silicon and germanium.

8. The construction of claim 1 wherein the transistor device is an NFET device.

9. The construction of claim 1 wherein the transistor device is a PFET device.

10. A semiconductor-on-insulator construction, comprising:

an electrically insulative material;

a monocrystalline layer comprising silicon and germanium over the electrically insulative material; and

an electrical device supported by the monocrystalline layer.

11. The construction of claim 10 wherein the electrically insulative material comprises silicon dioxide, and wherein the monocrystalline layer is in physical contact with the electrically insulative material.

12. The construction of claim 10 wherein the monocrystalline layer comprises from about 10 to about 60 atomic percent germanium.

13. The construction of claim 10 wherein the electrical device is a transistor and comprises a gate; wherein the monocrystalline layer has a relaxed crystalline lattice; and further comprising a strained crystalline lattice layer between the monocrystalline layer and the transistor gate.

14. The construction of claim 13 wherein the strained crystalline lattice layer is monocrystalline.

15. The construction of claim 13 wherein the strained crystalline lattice layer includes silicon.

16. The construction of claim 13 wherein the strained crystalline lattice layer includes silicon and germanium.

17. A semiconductor-on-insulator construction, comprising:

a substrate;

an insulator layer over the substrate;

a crystalline layer comprising silicon and germanium over the insulator layer; and

a transistor device supported by the crystalline layer, the transistor device comprising a gate and an active region proximate the gate; the active region including a channel region and a pair of source/drain regions; at least a portion of the active region being within the crystalline layer; an entirety of the active region within the crystalline layer being within a single crystal of the crystalline layer.

18. The construction of claim 17 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the crystalline layer and the transistor device gate.

19. The construction of claim 18 wherein the strained crystalline lattice layer includes silicon.

20. The construction of claim 19 wherein the transistor device is an NFET device.

21. The construction of claim 19 wherein the transistor device is a PFET device.

22. The construction of claim 18 wherein the strained crystalline lattice layer includes silicon and germanium.

23. The construction of claim 22 wherein the transistor device is a PFET device.

24. The construction of claim 17 wherein the insulator layer consists of silicon dioxide.

25. The construction of claim 17 wherein the entirety of the crystalline layer is a single crystal.

26. The construction of claim 17 wherein the crystalline layer is polycrystalline.

27. The construction of claim 17 wherein the crystalline layer is in physical contact with the insulator layer.

28. The construction of claim 17 wherein the crystalline layer consists of silicon and germanium.

29. The construction of claim 28 wherein the crystalline layer comprises from about 10 to about 60 atomic percent germanium.

30. The construction of claim 17 wherein the substrate comprises a semiconductive material.

31. The construction of claim 17 wherein the substrate comprises glass.

32. The construction of claim 17 wherein the substrate comprises aluminum oxide.

33. The construction of claim 17 wherein the substrate comprises silicon dioxide.

34. The construction of claim 17 wherein the substrate comprises a metal.

35. The construction of claim 17 wherein the substrate comprises a plastic.

36. A memory device comprising:

a transistor having a gate supported by a crystalline layer and having a pair of source/drain regions proximate the gate; the crystalline layer being less than or equal to about 2000 Å thick; the crystalline layer comprising a material which includes silicon and germanium; the transistor having an active region; at least a portion of the active region being within the material; the active region within the material being contained within a single crystal of the material; and

a capacitor electrically connected with one of the source/drain regions.

37. The memory device of claim 36 wherein the capacitor comprises:

a first electrode comprising n-type silicon;

a second electrode comprising n-type silicon; and

a dielectric material between the first and second electrodes.

38. The memory device of claim 37 wherein the dielectric material comprises one or more of silicon nitride, aluminum oxide, TiO_2, Ta_2O_5 and ZrO_2.

39. The memory device of claim 37 wherein the first electrode is connected to said one of the source/drain regions through an electrically conductive interconnect comprising n-type doped silicon.

40. The memory device of claim 39 wherein said one of the source/drain regions is n-type doped, and wherein the electrically conductive interconnect consists of n-type doped silicon.

41. The memory device of claim 36 wherein the crystalline layer is polycrystalline.

42. The memory device of claim 36 wherein the crystalline layer is monocrystalline.

43. The memory device of claim 36 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the crystalline layer and the transistor gate.

44. The memory device of claim 43 wherein the strained crystalline lattice includes silicon.

45. The memory device of claim 43 wherein the strained crystalline lattice includes silicon and germanium.

46. The memory device of claim 36 wherein the transistor is an NFET.

47. A computer system, the computer system comprising a memory device, the memory device including:

an array of memory cells, at least some of the memory cells including transistors having gates supported by a crystalline layer; the crystalline layer being less than or equal to about 2000 Å thick; the crystalline layer comprising a material which includes silicon and germanium; the at least some of the transistors having active regions within the crystalline layer; each active region within the crystalline layer including only one crystal of said material;

addressing circuitry coupled to the array of memory cells for accessing individual memory cells in the array of memory cells; and

a read circuit coupled to the memory cell array for reading data from memory cells in the array of memory cells.

48. The computer system of claim 47 wherein the memory device is selected from the group consisting of SDRAM, DDR SDRAM, SLDRAM, Direct RDRAM, SRAM, VRAM, EEPROM, and Flash memories.

49. The computer system of claim 47 wherein the crystalline layer is polycrystalline.

50. The computer system of claim 47 wherein the crystalline layer is monocrystalline.

51. The computer system of claim 47 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the crystalline layer and the transistor gates.

52. The computer system of claim 51 wherein the strained crystalline lattice includes silicon.

53. The computer system of claim 51 wherein the strained crystalline lattice includes silicon and germanium.

54. The computer system of claim 51 wherein the transistors have source/drain regions, and wherein the memory cells comprise capacitors connected to the transistors through the source/drain regions.

55. The computer system of claim 54 wherein the capacitors comprise electrodes consisting of n-type silicon.

56. The computer system of claim 55 wherein the electrodes are connected to the source/drain regions through electrically conductive interconnects comprising n-type doped silicon.

57. The computer system of claim 55 wherein the source/drain regions are n-type doped, and wherein the electrically conductive interconnects consist of n-type doped silicon.

58. The computer system of claim 54 wherein the capacitors comprise:

first electrodes comprising n-type silicon;

second electrodes comprising n-type silicon; and

dielectric material between the first and second electrodes.

59. The computer system of claim 58 wherein the dielectric material comprises one or more of silicon nitride, aluminum oxide, TiO_2, Ta_2O_5 and ZrO_2.

60. The computer system of claim 58 wherein the first electrodes are connected to the source/drain regions through electrically conductive interconnects comprising n-type doped silicon.

61. The computer system of claim 60 wherein the source/drain regions are n-type doped, and wherein the electrically conductive interconnects consist of n-type doped silicon.

62. A process of forming a semiconductor-on-insulator construction, comprising:

forming a first layer over a substrate, the first layer being electrically insulative;

forming a plurality of discrete islands of material over the first layer;

forming crystals in the material of the discrete islands;

forming a second layer over the discrete islands, the second layer comprising silicon and germanium;

forming metal in physical contact with the second layer; and

utilizing the metal for metal-induced-lateral-recrystallization of the second layer, the metal-induced-lateral-recrystallization converting the second layer to a crystalline material.

63. The method of claim 62 wherein the crystalline material consists of a single crystal.

64. The method of claim 62 wherein the crystalline material is polycrystalline.

65. The method of claim 62 further comprising removing the metal from over the crystalline material.

66. The method of claim 62 wherein the substrate comprises one or more of glass, semiconductive material, metal, plastic, SiO_2 and Al_2O_3.

67. The method of claim 62 wherein the first layer consists of silicon dioxide.

68. The method of claim 62 wherein the material of the discrete islands consists of silicon or doped silicon.

69. The method of claim 62 wherein the material of the discrete islands consists of doped silicon in which the dopant concentration is from about 10^{14} atoms/cm^3 to about 10^{20} atoms/cm^3.

70. The method of claim 62 wherein the discrete islands have a thickness of from about 5 nanometers to about 10 nanometers.

71. The method of claim 62 wherein the second layer consists of silicon and germanium.

72. The method of claim 62 wherein the second layer consists of silicon, germanium and one or more dopants.

73. The method of claim 62 wherein the second layer has a thickness of from about 50 nanometers to about 100 nanometers.

74. The method of claim 62 wherein the metal comprises nickel.

75. The method of claim 62 wherein the forming the crystals in the material of the discrete islands comprises implanting helium into said material to form voids and subsequently exposing said material to laser-emitted electromagnetic radiation to form the crystals.

76. The method of claim 75 further comprising forming a cap over the discrete islands prior to implanting the helium, and removing the cap prior to forming the second layer.

77. The method of claim 76 wherein the cap comprises silicon dioxide.

78. The method of claim 62 further comprising converting at least a portion of one or more of the islands to silicon dioxide after forming the second layer and prior to the metal-induced-lateral-recrystallization.

79. The method of claim 78 wherein the converting comprises implanting O_2 into said one or more of the islands.

80. The method of claim 62 further comprising:

forming a third layer over the second layer;

removing portions of the third layer to form openings extending through the third layer to the second layer; and

forming the metal within the openings.

81. The method of claim 80 wherein the third layer comprises silicon dioxide.

82. A process of forming a transistor associated with a semiconductor-on-insulator construction, comprising:

forming a first layer over a substrate, the first layer being electrically insulative;

forming a plurality of discrete islands of material over the first layer;

exposing the material of the discrete islands to helium and laser-emitted electromagnetic radiation;

forming a second layer over the discrete islands, the second layer comprising silicon and germanium;

forming metal in physical contact with the second layer and utilizing the metal for metal-induced-lateral-recrystallization of the second layer, the metal-induced-lateral-recrystallization converting the second layer to a crystalline material;

forming a transistor gate over the crystalline material;

forming a pair of source/drain regions gatedly connected to one another by the gate and extending into the crystalline material.

83. The method of claim 82 wherein the forming the source/drain regions comprises implanting dopant into the crystalline material.

84. The method of claim 82 wherein the crystalline material has a relaxed crystalline lattice, and further comprising:

forming a strained crystalline lattice over the relaxed crystalline lattice; and

forming the transistor gate over the strained crystalline lattice.

85. The method of claim 84 wherein the strained crystalline lattice and relaxed crystalline lattice together define a crystalline mass having a thickness of less than or equal to 2000Å.

86. The method of claim 84 wherein the strained crystalline lattice includes silicon.

87. The method of claim 84 wherein the strained crystalline lattice includes silicon and germanium.

88. The method of claim 82 wherein the transistor gate and source/drain regions are comprised by an NFET device.

89. The method of claim 82 wherein the transistor gate and source/drain regions are comprised by a PFET device.

90. The method of claim 82 wherein the transistor gate and source/drain regions are associated with an active region which extends into the crystalline material, and wherein an entirety of the active region within the crystalline material is within only a single crystal of the crystalline material.

91. A method of forming a memory device, comprising:

forming a buffer layer over a substrate;

forming a first crystalline layer over the buffer layer; the first crystalline layer having a relaxed crystalline lattice and comprising silicon and germanium;

forming a second crystalline layer over the first crystalline layer, the second crystalline layer having a strained crystalline lattice;

forming a transistor gate over the second crystalline layer;

forming a pair of source/drain regions proximate the gate and extending into the first and second crystalline layers; the transistor gate and source/drain regions together being comprised by a transistor; and

forming a capacitor electrically connected with one of the source/drain regions.

92. The method of claim 91 wherein the first crystalline layer is monocrystalline.

93. The method of claim 91 wherein the first crystalline layer is polycrystalline.

94. The method of claim 91 wherein the second crystalline layer is monocrystalline.

95. The method of claim 91 wherein the second crystalline layer is polycrystalline.

96. The method of claim 91 wherein the first and second crystalline layers together have a thickness of less than or equal to about 2000Å.

97. The method of claim 91 wherein the transistor has an active region extending through the second crystalline layer and into the first crystalline layer; the active region thus having a portion within the first crystalline layer; the portion of the active region within the first crystalline layer including only one single crystal of the first crystalline layer.

98. The method of claim 91 wherein the strained crystalline lattice includes silicon; and wherein crystalline grains of the strained crystalline lattice are in a one-to-one correspondence with crystalline grains of the relaxed crystalline lattice.

99. The method of claim 91 wherein the strained crystalline lattice includes silicon and germanium; and wherein crystalline grains of the strained crystalline lattice are in a one-to-one correspondence with crystalline grains of the relaxed crystalline lattice.

100. The method of claim 91 wherein the forming the capacitor comprises:

forming a first electrode comprising n-type silicon:

forming a dielectric material over the first electrode; and

forming a second electrode comprising n-type silicon over the dielectric material.

101. The method of claim 100 wherein the dielectric material comprises one or more of silicon nitride, aluminum oxide, TiO_2, Ta_2O_5 and ZrO_2.